17659

16117

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Use of Non-programmable Electronic Pocket Calculator is permissible.

(7) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

(8) Use of Steam tables, logarithmic, Mollier's chart is permitted.

Marks

1. a) **Attempt any THREE of the following:** **12**

(i) Explain the process of estimation of resistance of the channel and how it is calculated.

(ii) Draw NAND and NOR gates using NMOS.

(iii) Explain Latch-up in CMOS and how it is minimized.

(iv) Explain any three operators used in VHDL.

b) **Attempt any ONE of the following:** **6**

(i) Explain CZ process for wafer fabrication, with neat diagram.

(ii) Define the terms:

1) Metastability

2) Noise margins

3) Skew

Marks

2. Attempt any FOUR of the following: **16**

a) Differentiate between Xiliv and Atmel series architecture of CPLD. (four points)

b) Compare Moore and Mealy machines. (four points)

c) Write VHDL code for 3-bit up-counter.

d) What are the advantages of twin-tub process of CMOS fabrication?

e) List the types of FSM. Draw labelled diagram of each.

f) Write the advantages and purpose of VHDL.

3. Attempt any FOUR of the following: **16**

a) Explain basic architecture of sparton 3 FPGA series.

b) What is Test bench and write down a typical test bench format.

c) Write VHDL code to implement 4:1 multiplexer.

d) Draw NAND gate using CMOS transistors.

e) Explain P well process with suitable diagram.

f) Write the output equation of Moore and Mealy machines. List any two examples of FSM.

4. a) Attempt any THREE of the following: **12**

(i) Write VHDL code to implement 4-bit adder.

(ii) Explain the following terms

1) Event scheduling

2) Simulation cycle

(iii) Draw CMOS transistor fabrication using n-well process.

(iv) Explain the following terms

1) Architecture

2) Configuration

b) Attempt any ONE of the following: **6**

(i) Draw architecture of XC9500 CPLD.

(ii) Design a sequence detector to detect the sequence 101.

Marks

5. Attempt any FOUR of the following: **16**

a) Differentiate FPGA and CPLD.

b) List and explain data types used in HDL.

c) Explain in cycle based simulation.

d) Draw the CMOS inverter characteristic and explain it.

e) Explain shift operators with example.

f) What is event scheduling and zero modelling.

6. Attempt any FOUR of the following: **16**

a) Explain oxidation and diffusion process in fabrication process.

b) Define the following terms related to VHDL

(i) Package

(ii) Entity

c) Explain HDL design flow for synthesis.

d) Explain the following terms

(i) Delta Delay

(ii) Sensitivity list

e) Execute the following equation by the circuit with CMOS logic.

$D = [(A \cdot B) + (C \cdot D)]$

f) What is meant by efficient coding style? How arithmetic expressions are optimized?